

FIG. 1 PRIOR ART

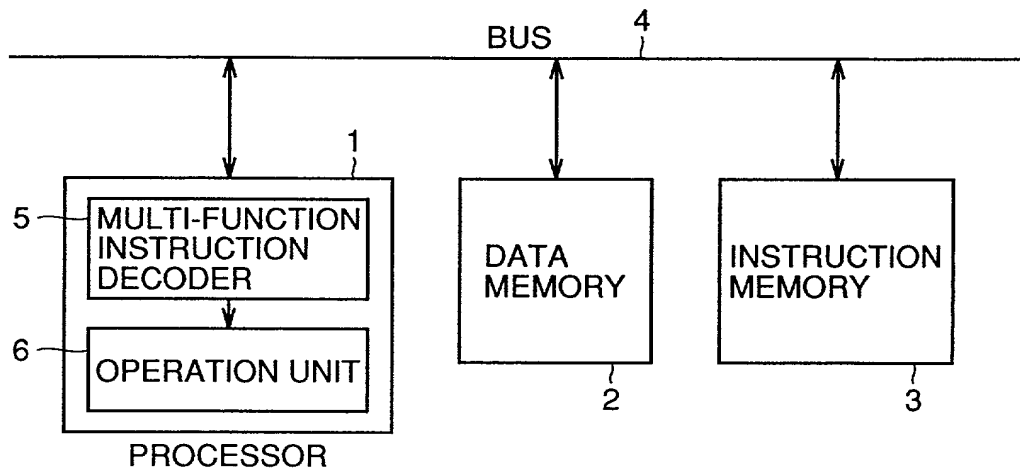


FIG.2

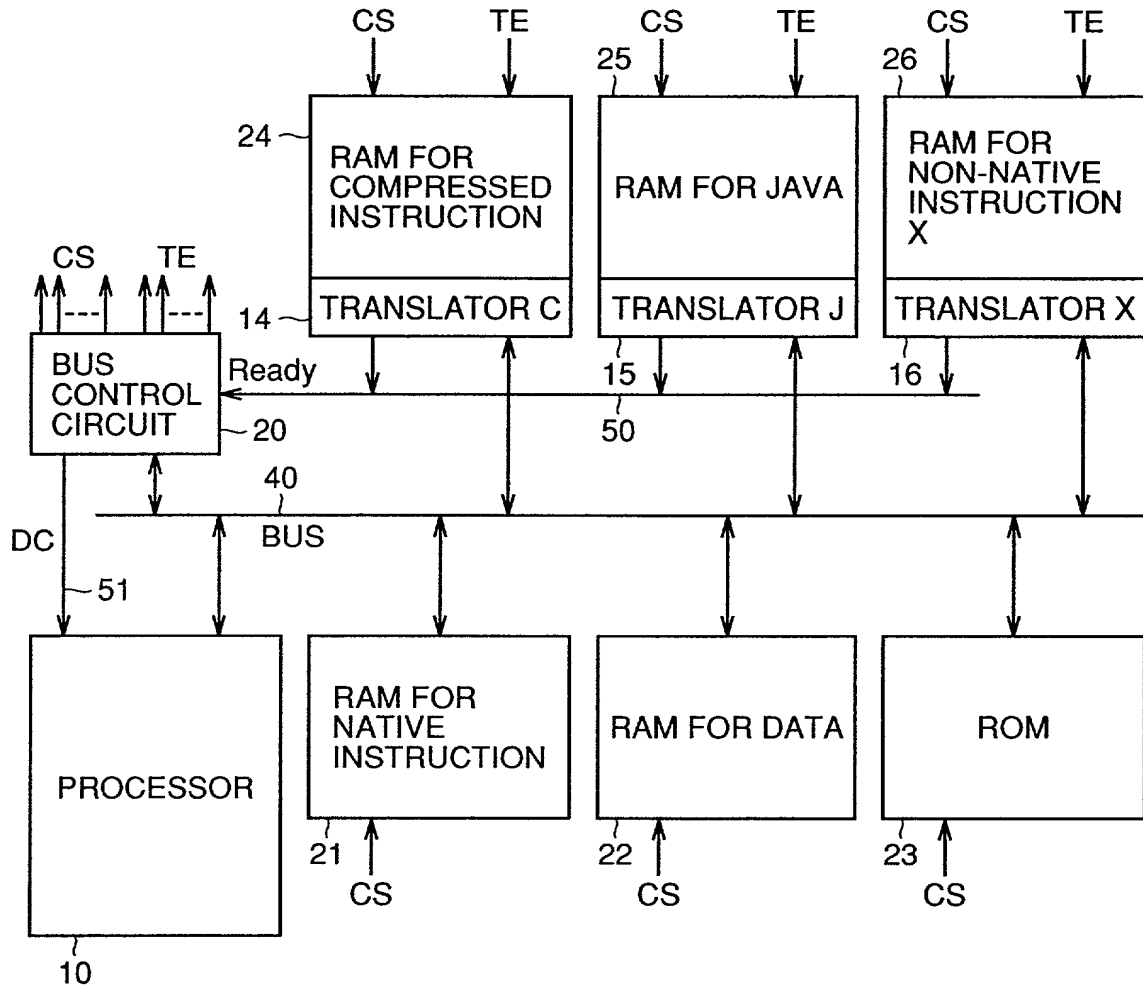


FIG.3

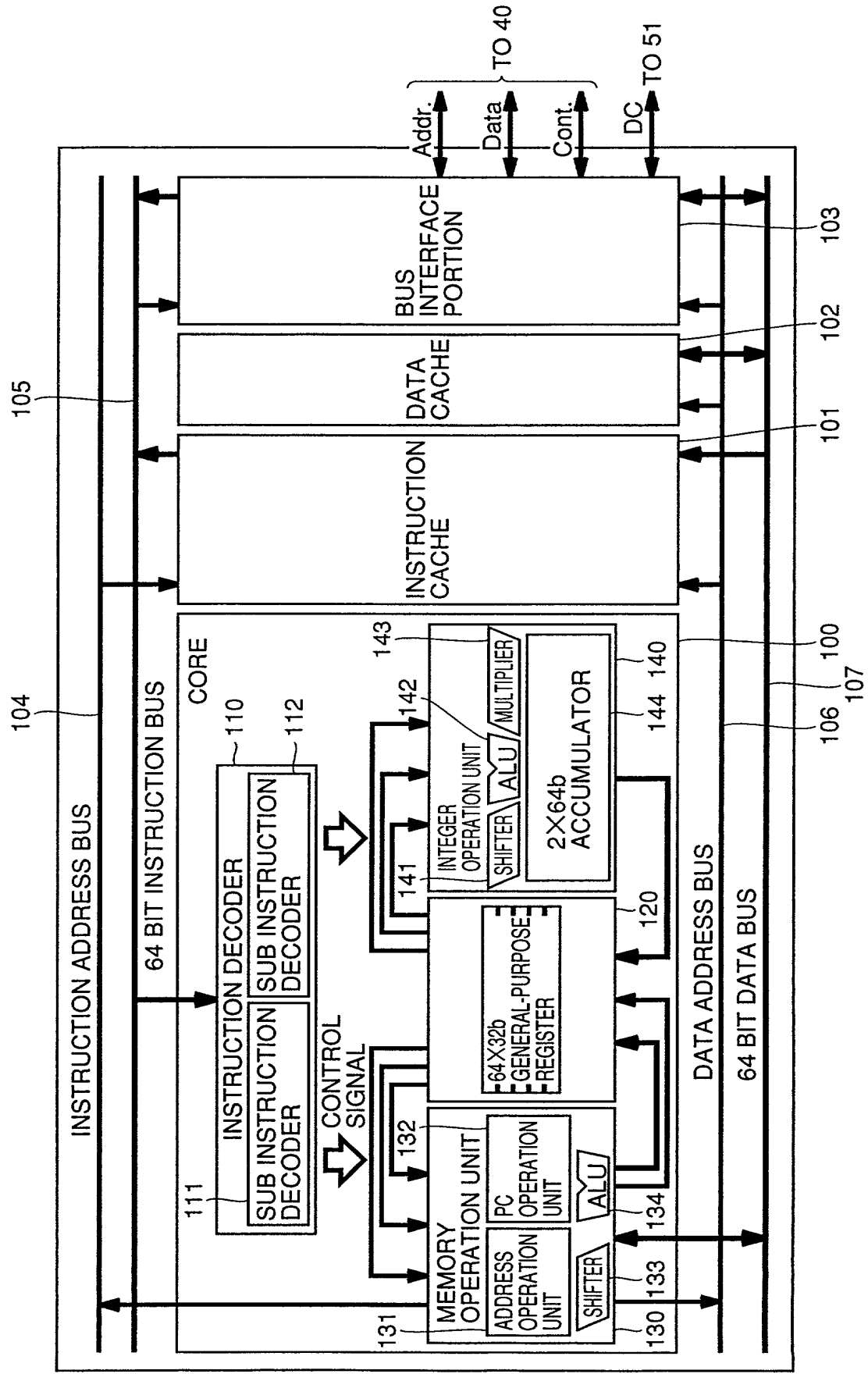


FIG.4

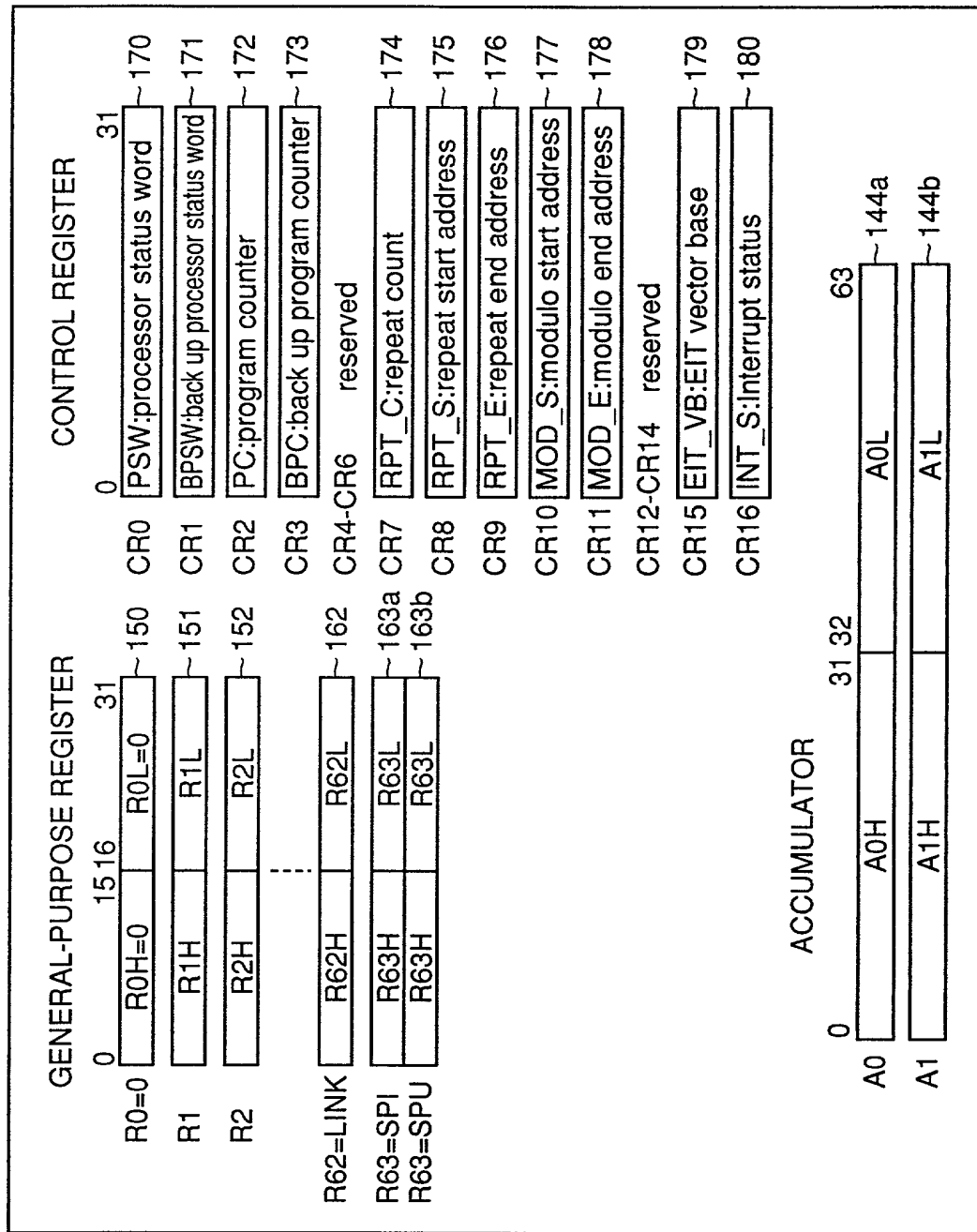


FIG.5

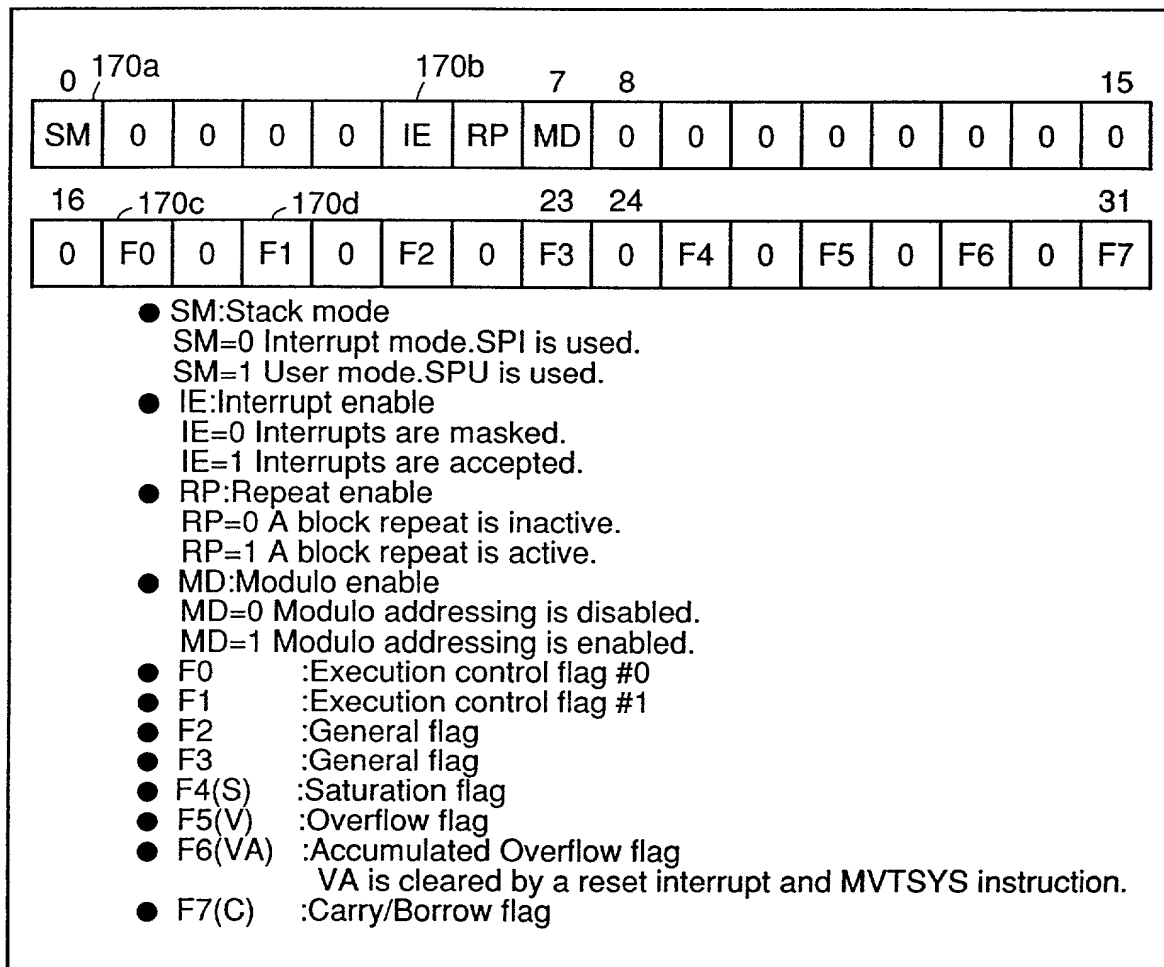


FIG.6

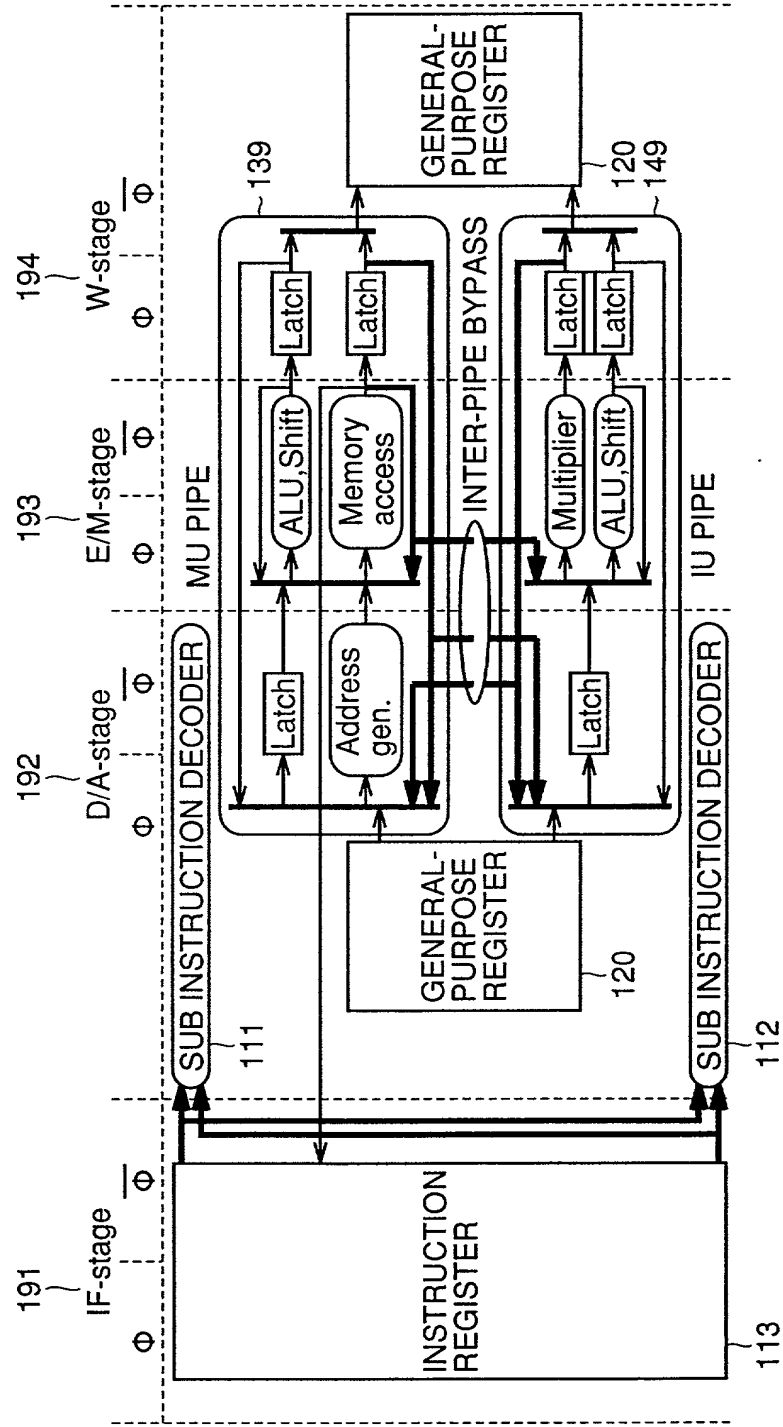


FIG. 7

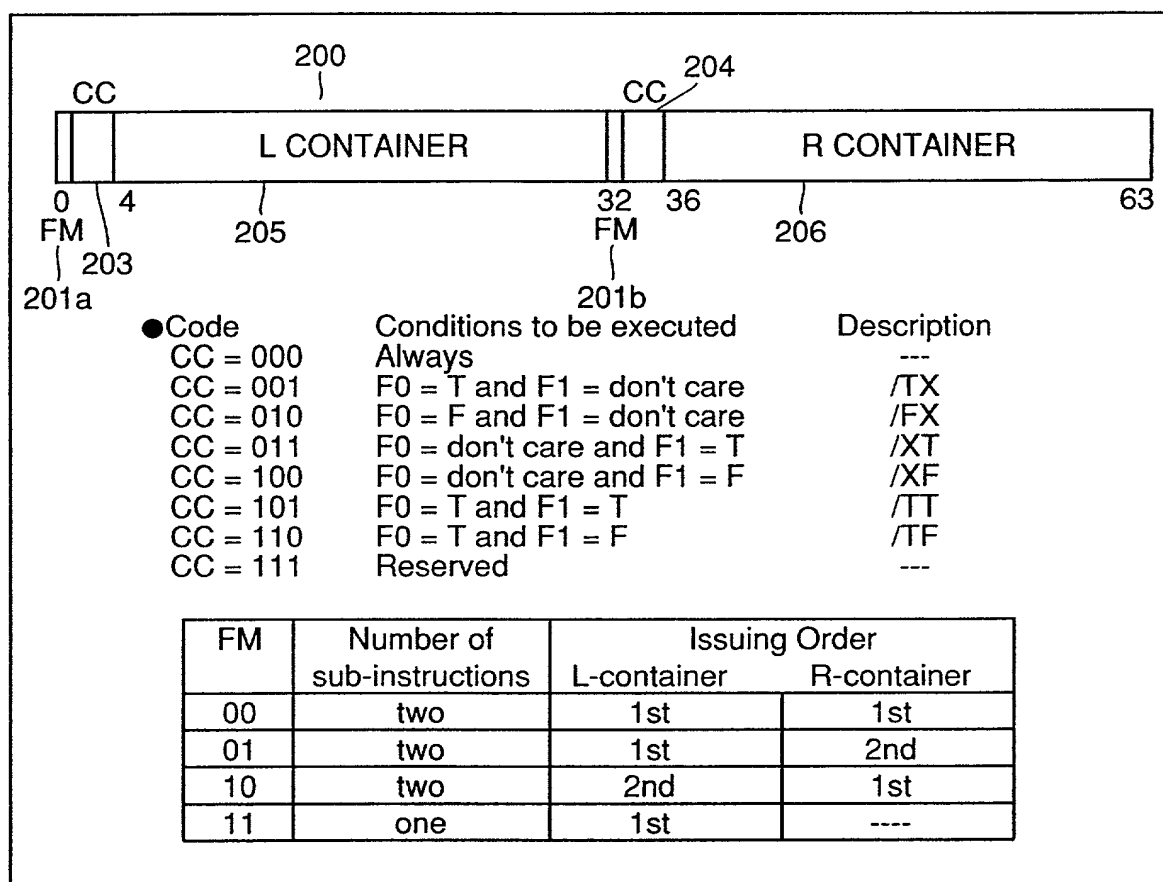


FIG.8

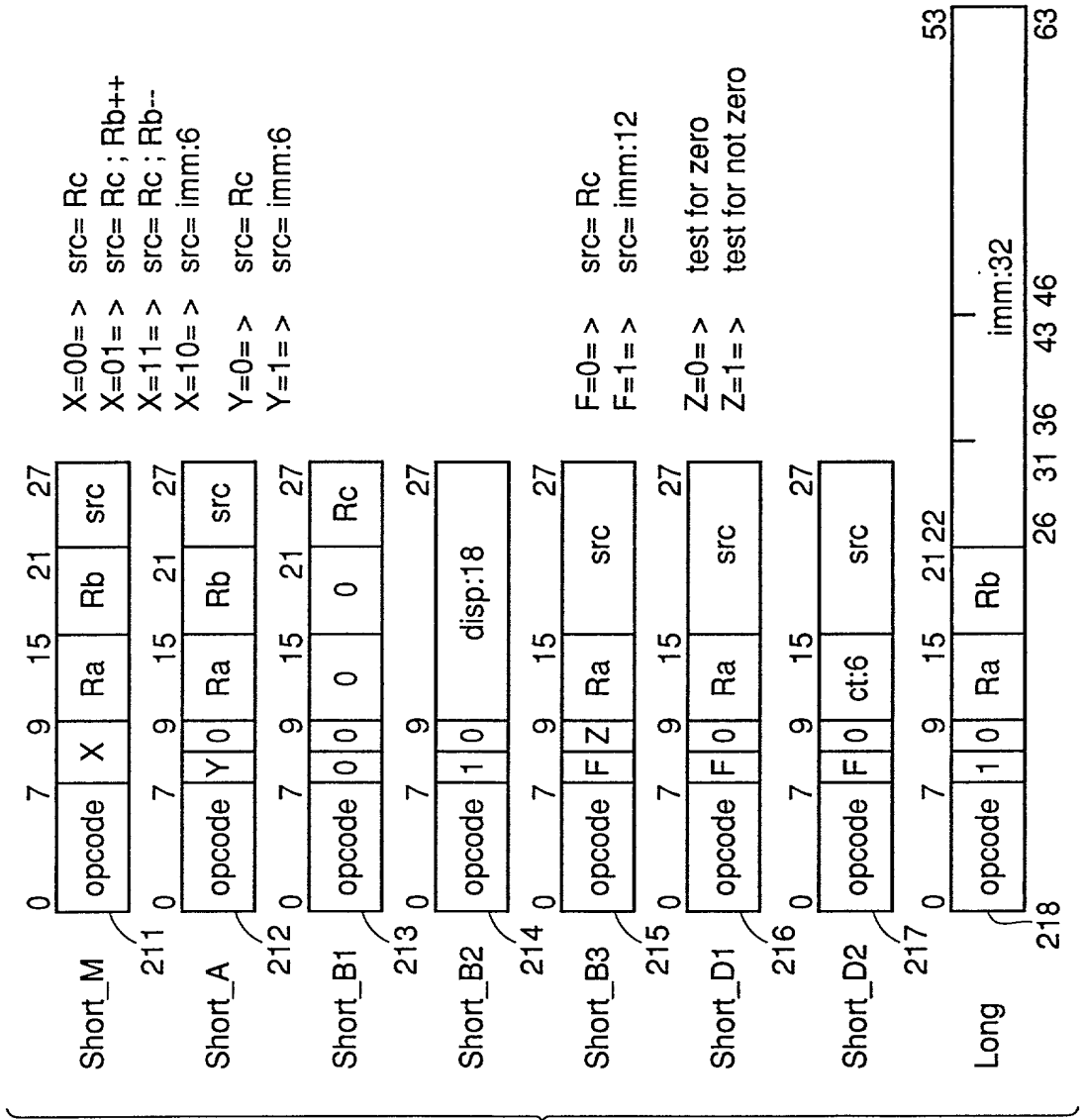


FIG.9

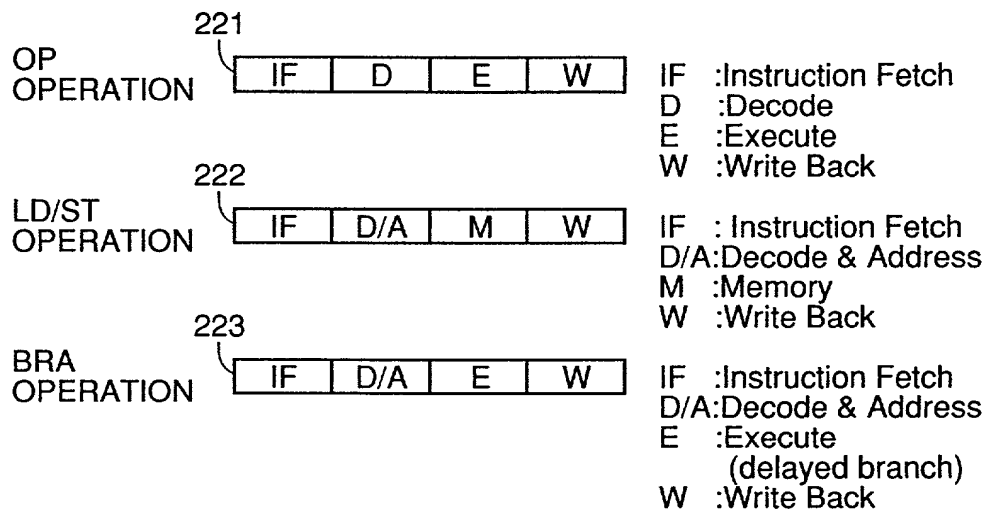


FIG.10

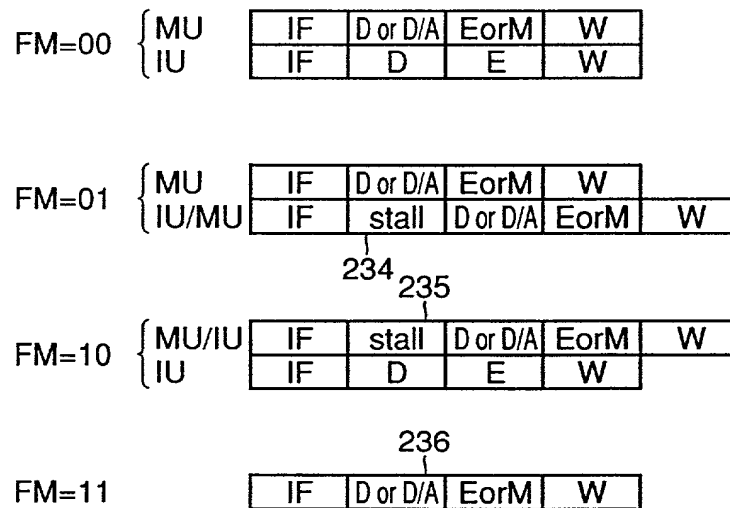


FIG. 11

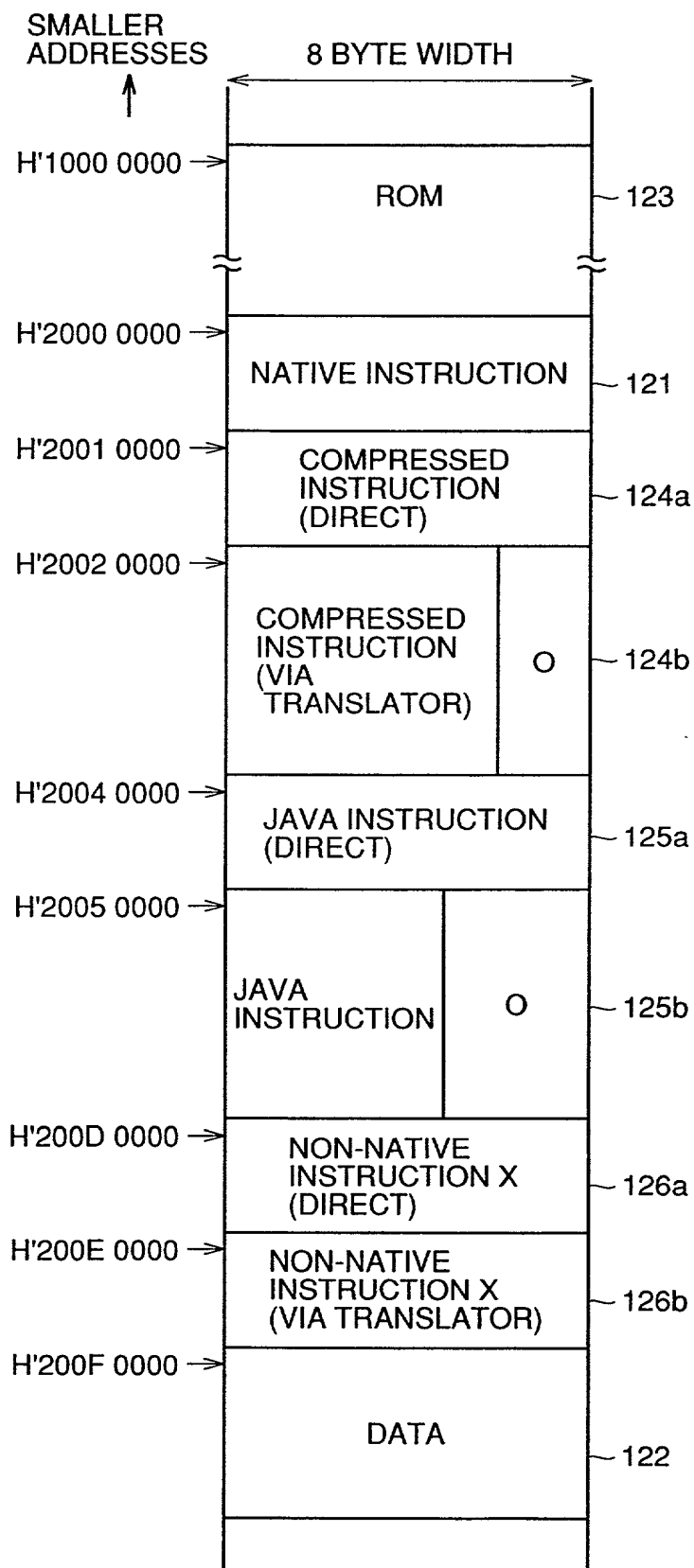


FIG. 12

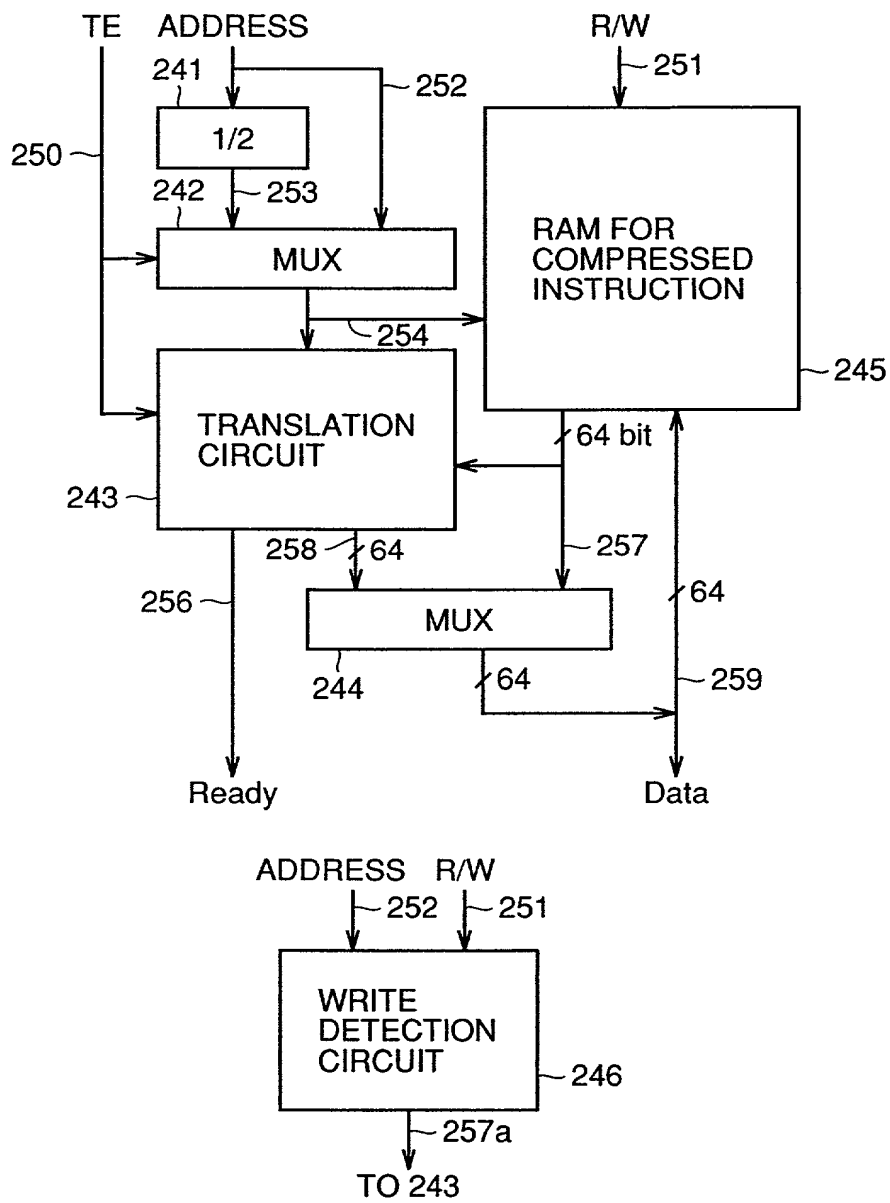


FIG. 14

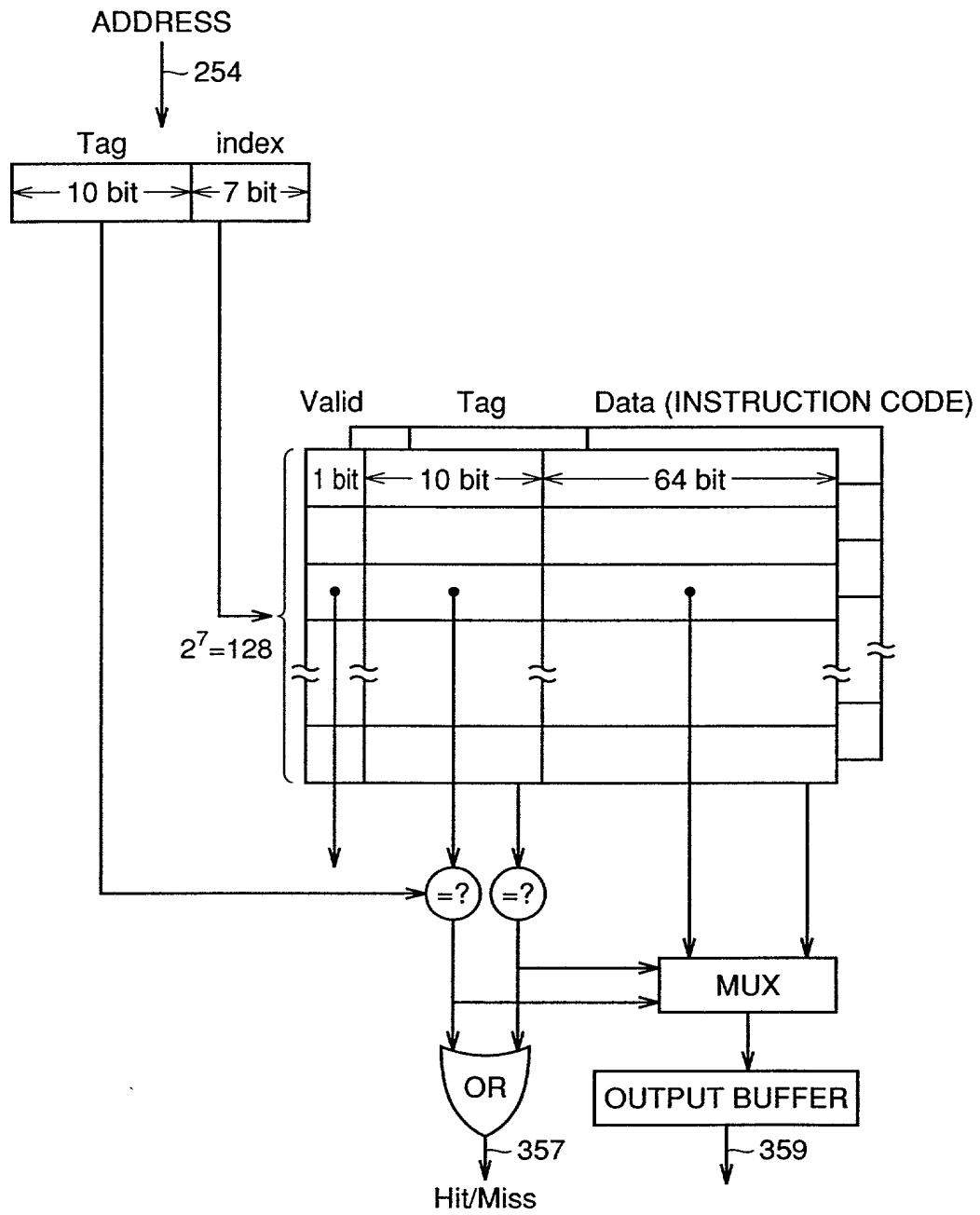


FIG.15

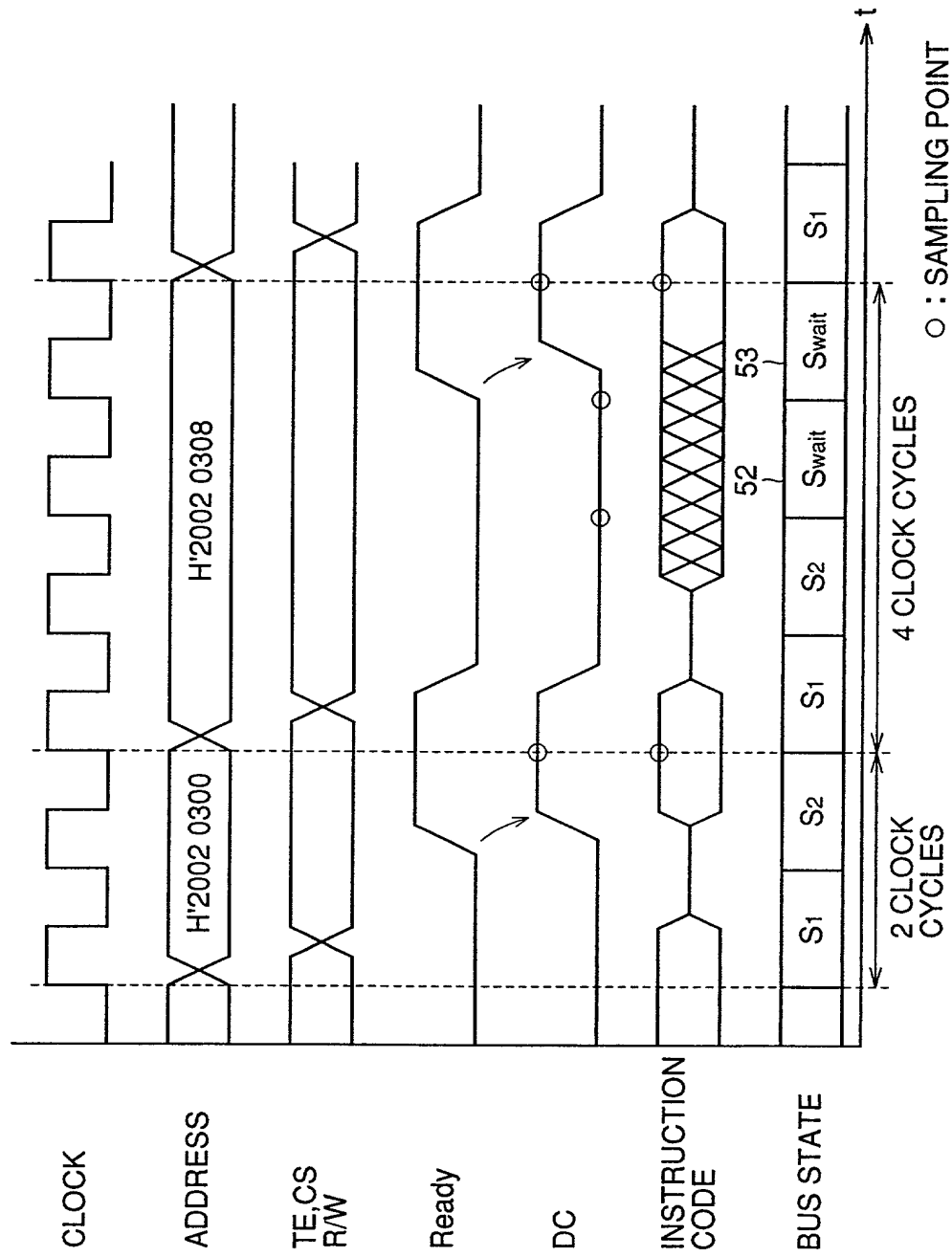


FIG.16

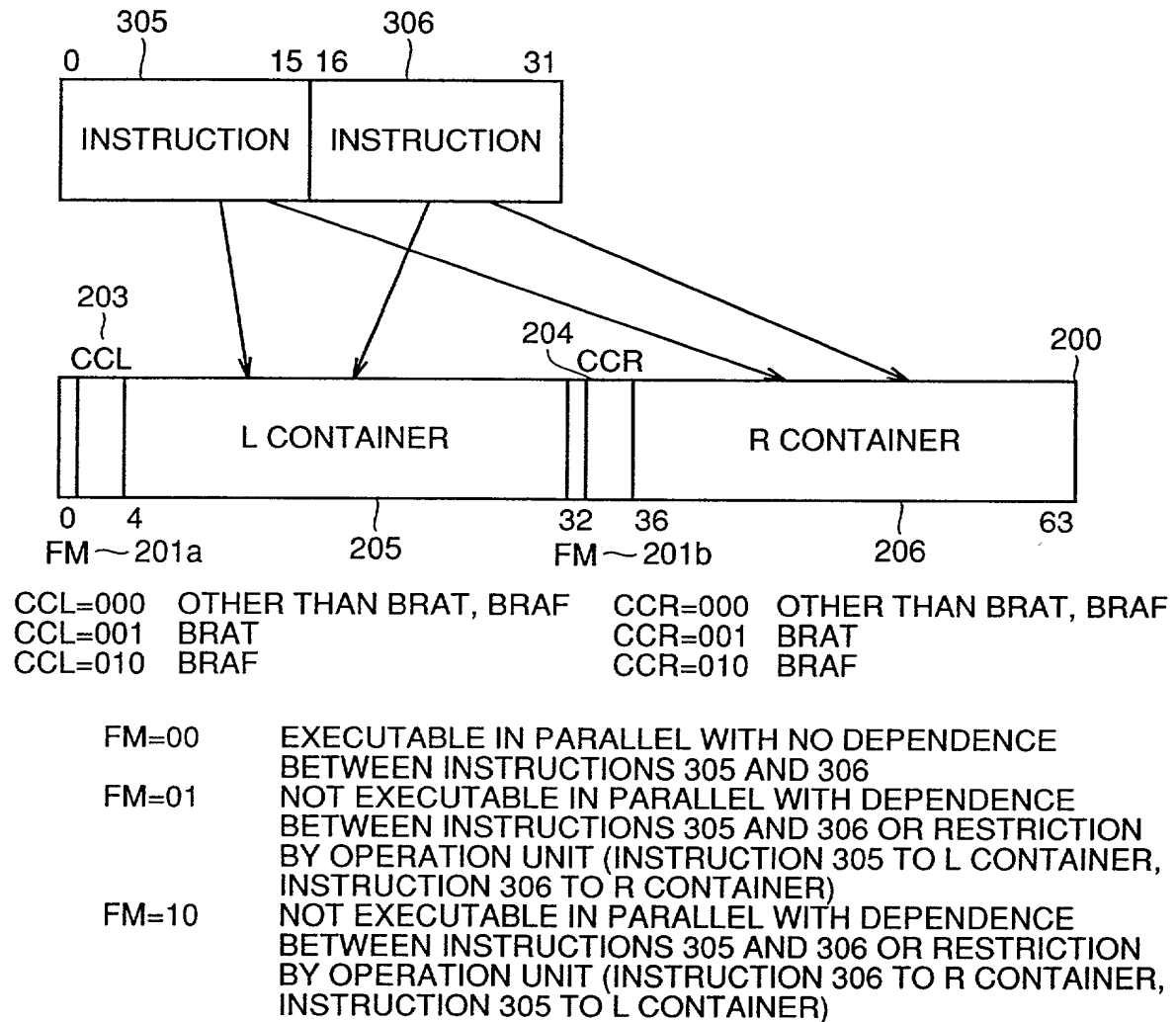


FIG.17

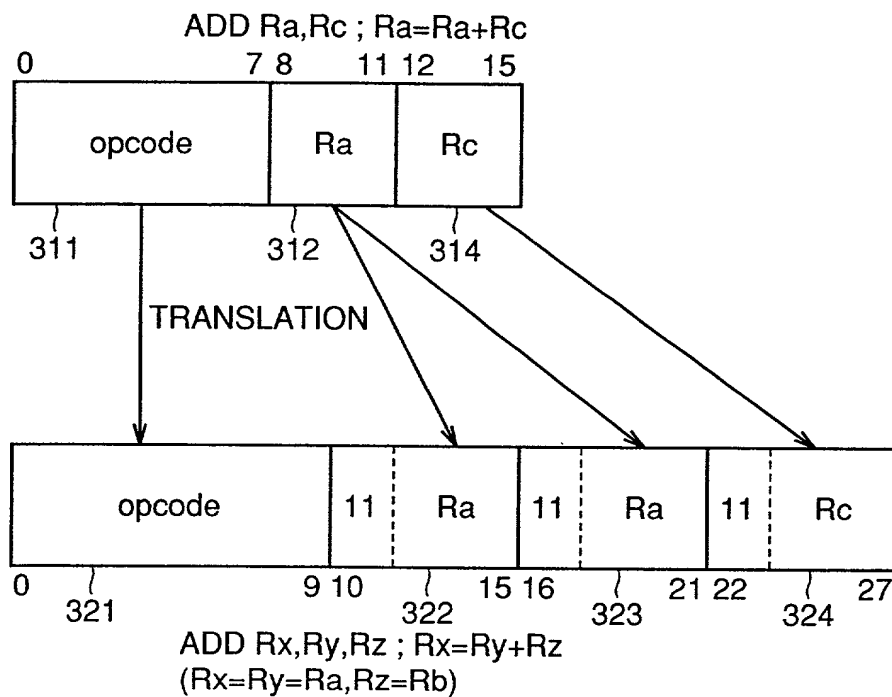


FIG.18

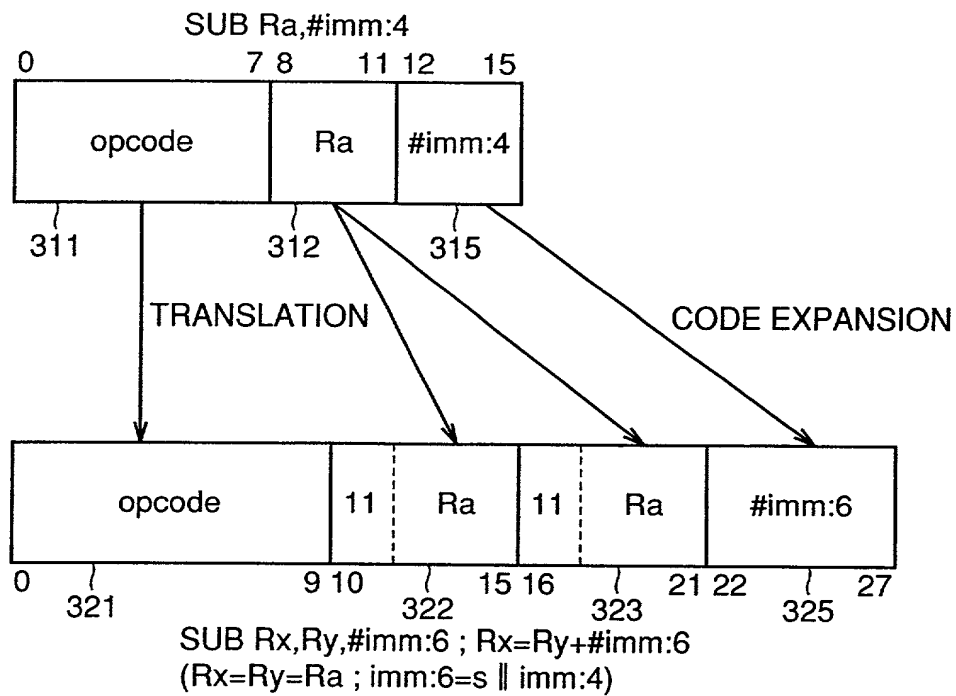


FIG.19

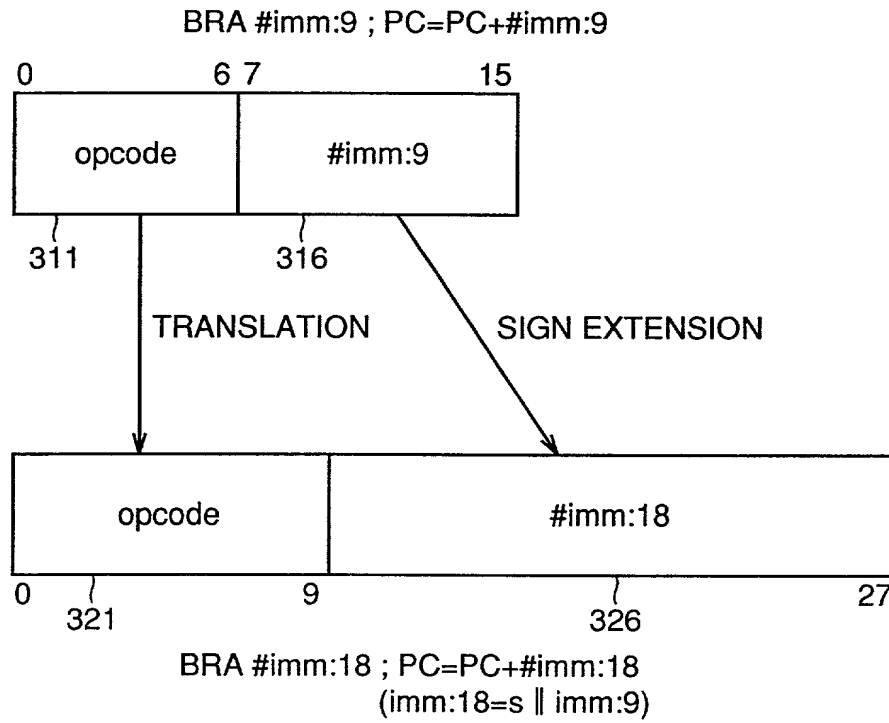


FIG.20

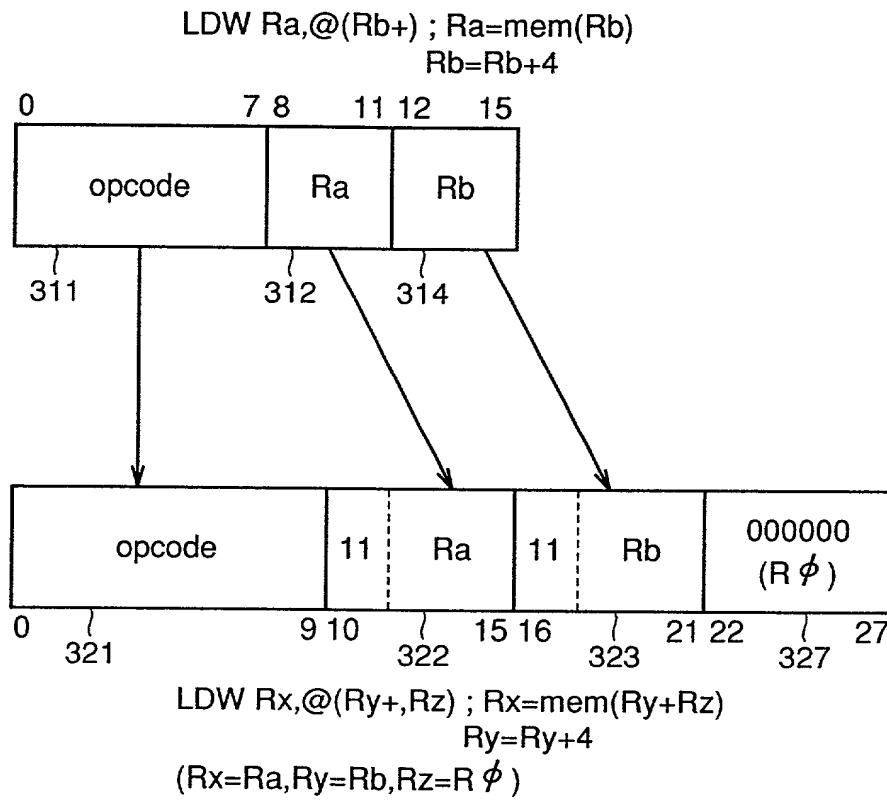
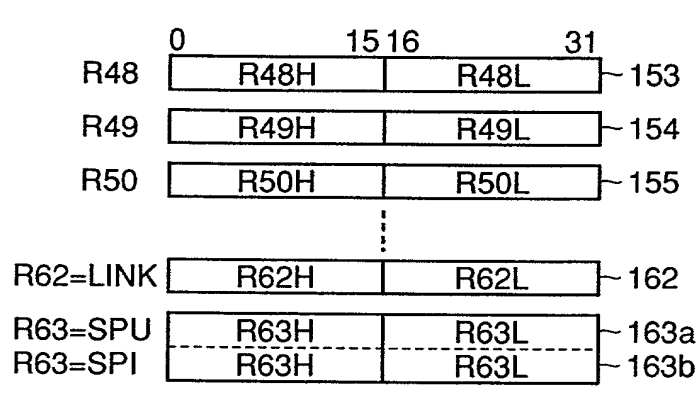


FIG.21



(continued)

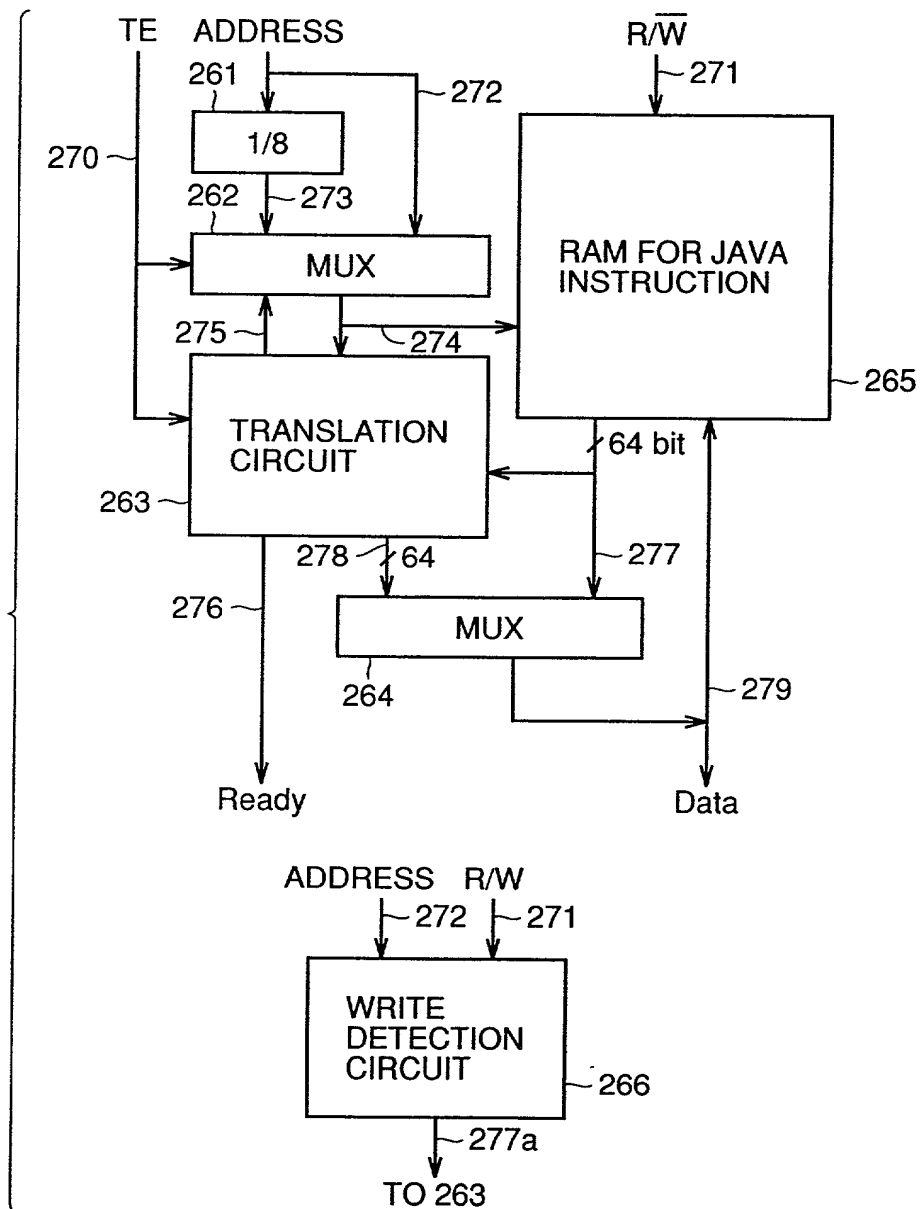
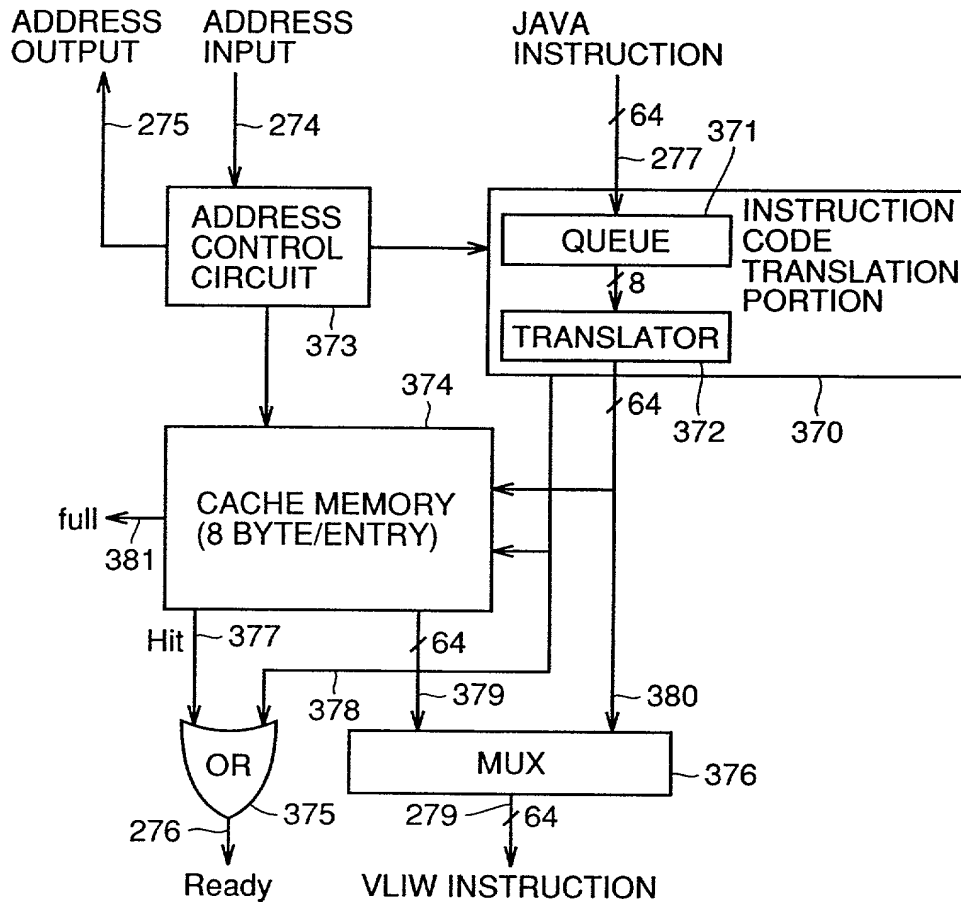


FIG.23



TRANSLATION CIRCUIT

FIG.24

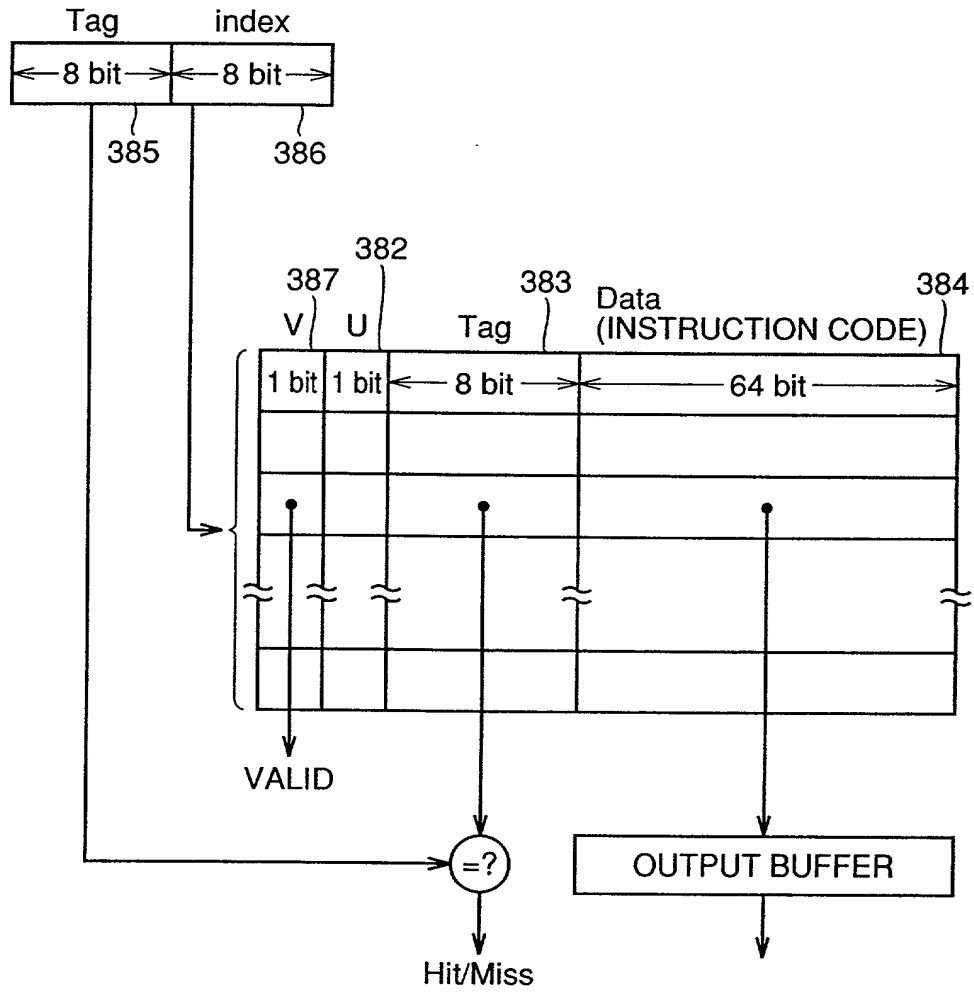


FIG.25

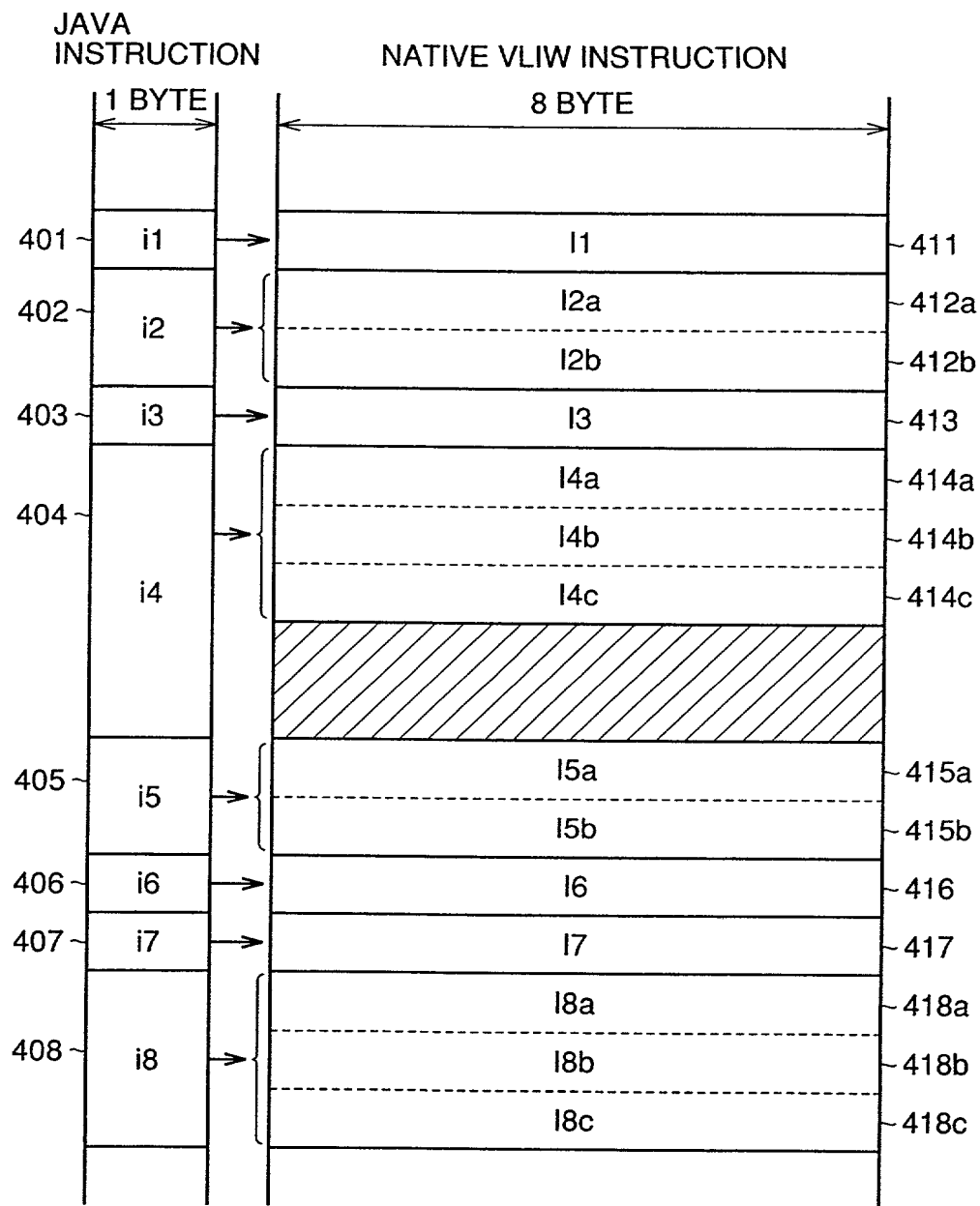
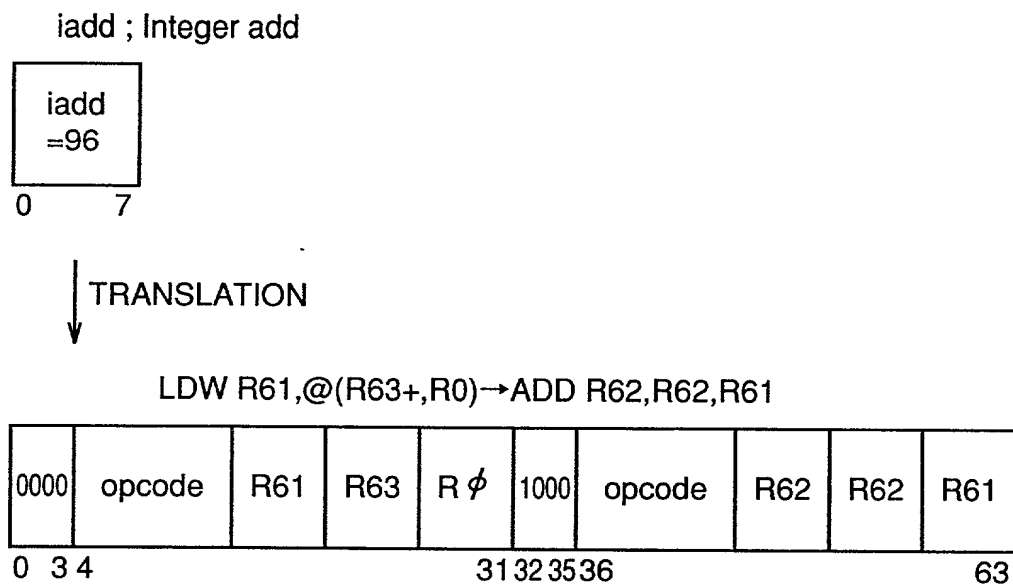
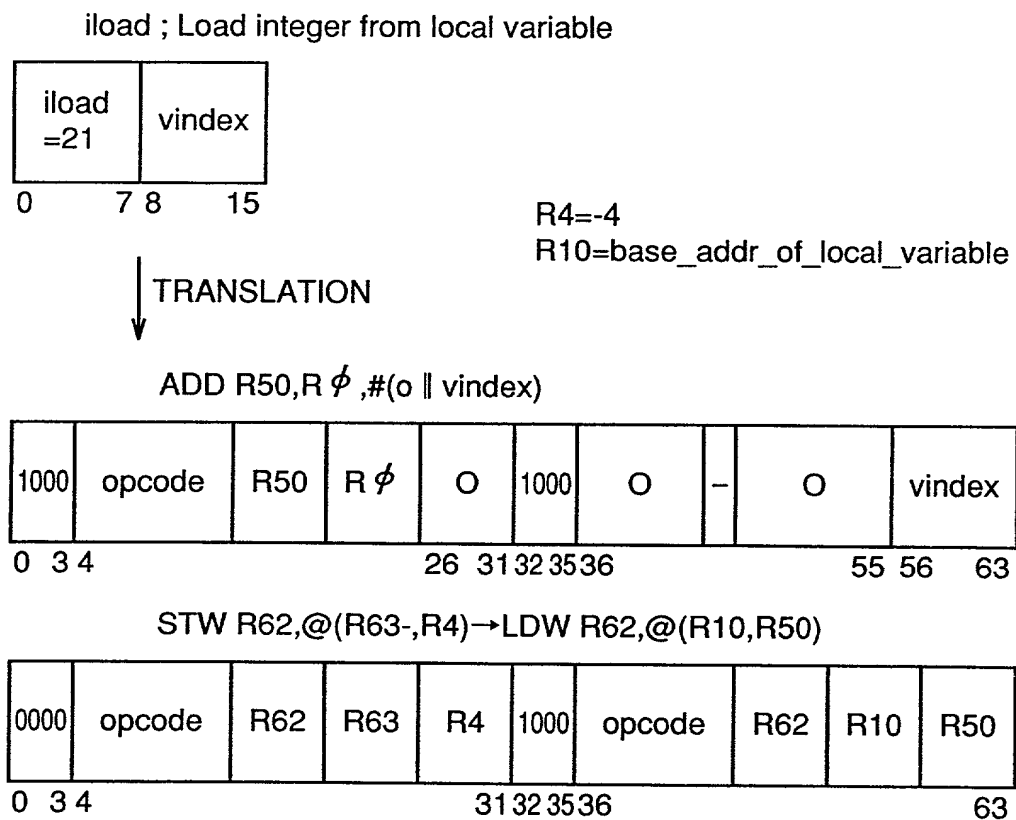


FIG.26



EXAMPLE OF 1BYTE → 1 VLIW INSTRUCTION

FIG.27



EXAMPLE OF 2 BYTE → 2 VLIW INSTRUCTION

FIG.28

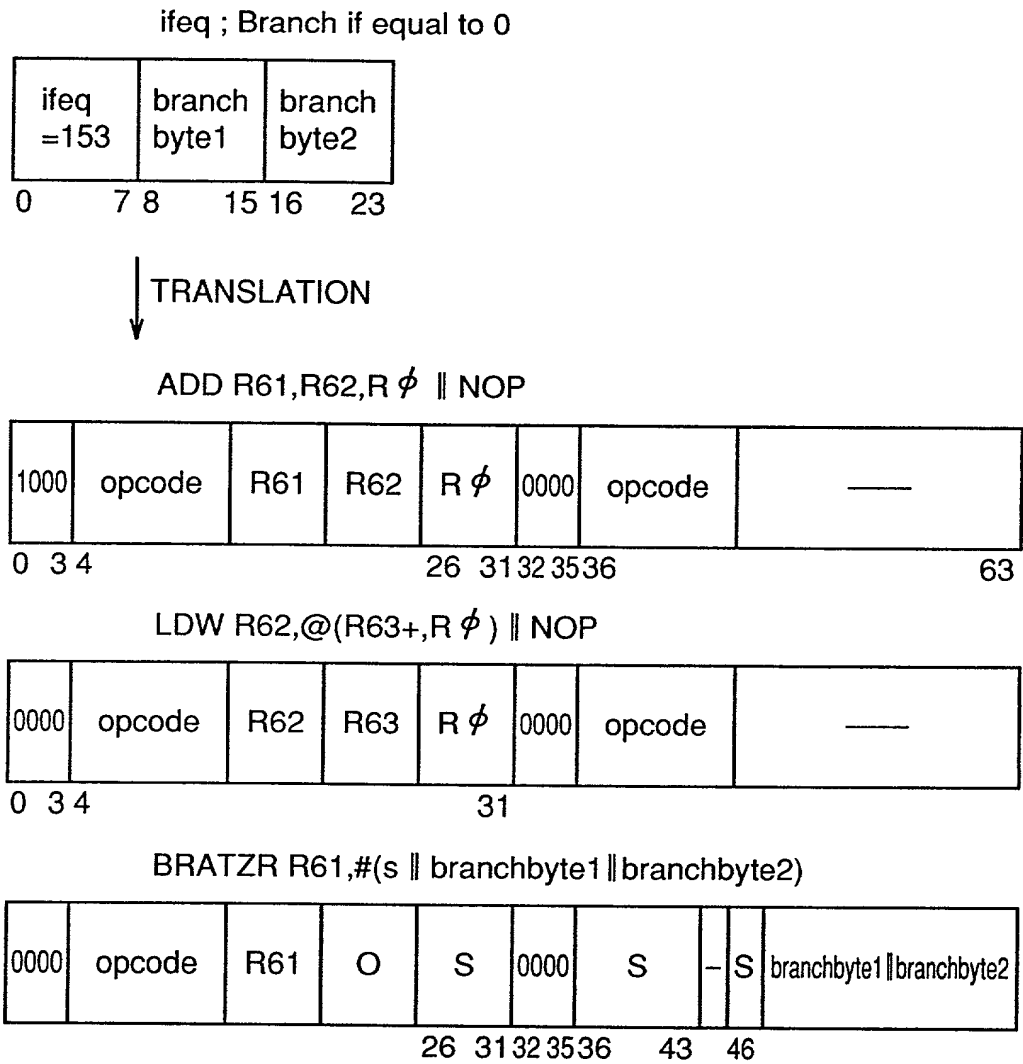


FIG.29

jsr_w ; Jumpto subroutine (wide index)

goto_w =200	branch byte1	branch byte2	branch byte3	branch byte4
0 7 8	15 16	23 24	31 32	39

TRANSLATION
↓

OR R10,R0,#(branchbyte1 || branchbyte2 || branchbyte3 || branchbyte4)

1000	opcode	—	bb0	1000	bb1	—	bb2	branch byte3	branch byte4
0 3 4			26 31 32 35 36	43	46				63

STW R62,@(R63-,R4)→JSR R10

0000	opcode	R62	R63	R4	1000	opcode	—	R10
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BRA #3 || NOP

0000	opcode	#3	000 0000	opcode	—
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FIG.30

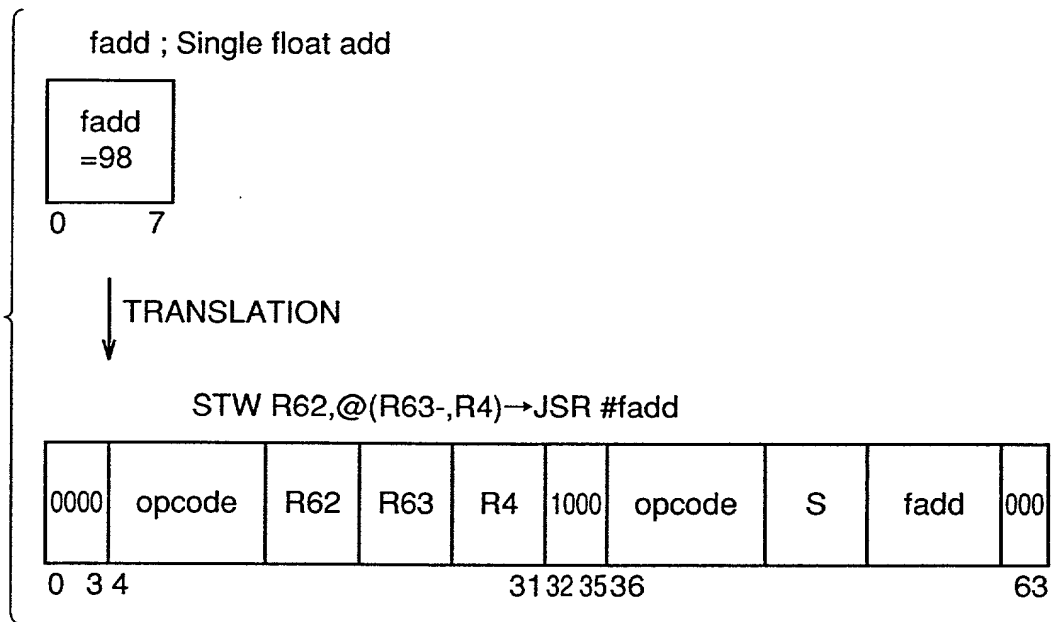


FIG.31

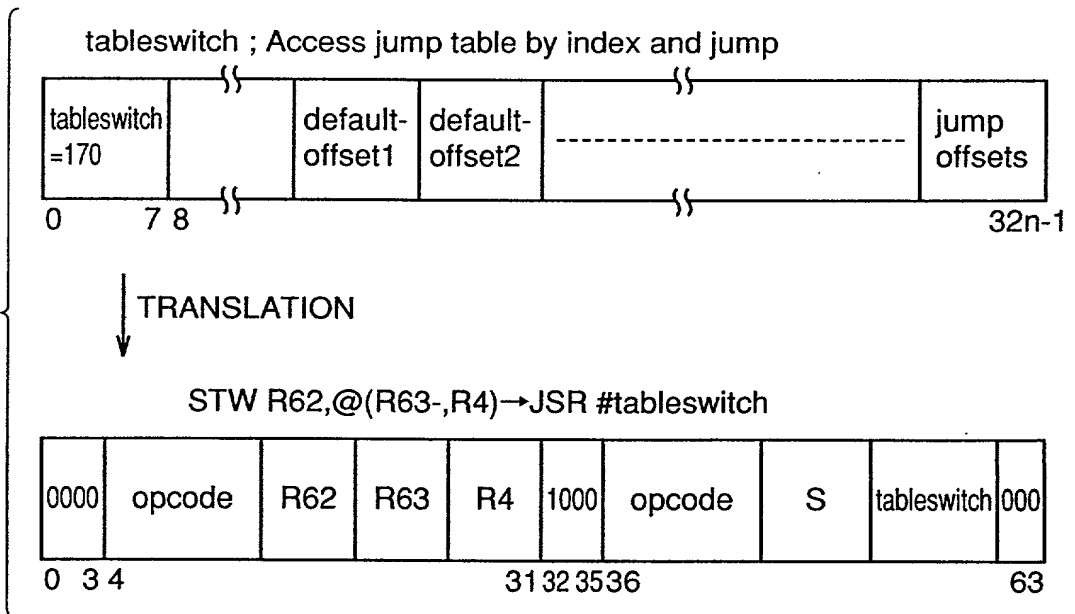


FIG.32

